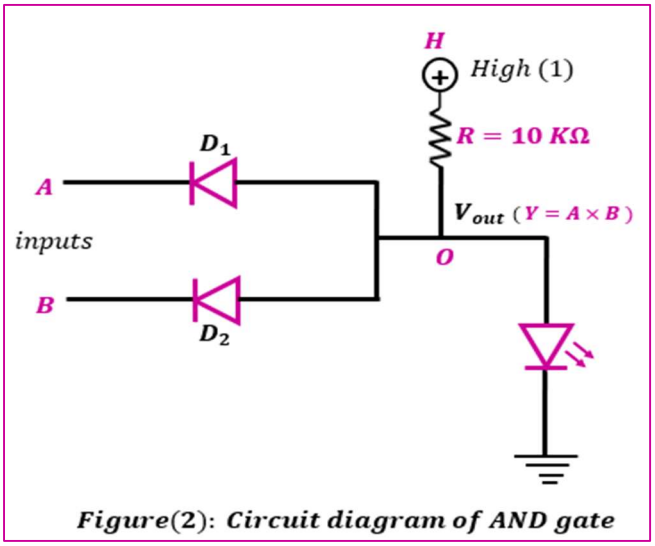
Circuit diagram and operation of AND gate:

The circuit diagram of an AND gate is as shown in figure (2). The circuit has two diodes (D_1 *and* D_2), a light emitting diode (LED) and a resistor (R) in series with $+ve$ terminal of a cell.

Here, A and B are inputs and Y is output.



Figure(2): *Circuit diagram of AND gate*

Operation:

The point H is always connected to $+ve$ terminal of a cell (High supply).

1. When the value of both inputs A and B is low (0 Volt), both diodes $D_1$and D_2 are forward biased. In this situation, both the diodes conduct and then the value of output becomes zero. Resultantly, point O (output) becomes zero.
   Potential is dropped across R and hence no potential is achieved at point O.
2. When input A is low and B is high, the diode D_1 becomes forward biased and the diode D_2 is reverse biased. In this situation the value of output become zero (due to conducting of D_1). Resultantly, point O (output) becomes zero.
3. Similarly, when input A is high and B is low, the diode D_2 becomes forward biased and the diode D_1 is reverse biased. In this situation the value of output become zero (due to conducting of D_2). Resultantly, point O (output) becomes zero.
4. When value of both the inputs A and B is high ($+5V$), both the diodes are reverse biased. In this situation, neither diode conduct and no supply current passes through R. Thus, no voltage drop takes place across R. Hence, Potential is achieved at point O (output).

   In other words, when both of the inputs are high (i. e. +5V), both the diodes do not conduct (both being reverse biased). Therefore, a high output is achieved.

Thus, in an AND gate, the output is high only when both the inputs are high and the output is low if any of the inputs are low.

PROCEDURE:

For OR gate:

1. Connect the circuit as in figure- with two different inputs and a common output.
2. When input A is at +V, the D_1 is forward biased and hence conducts. The circuit current flows via R dropping +V across it (almost V) and hence yields high output (Y).
3. When input B is at +V, the D_2 is forward biased and hence yields high output.
4. Similarly, when both inputs A and B are at +V, both diodes are forward biased and hence conduct. Again, the output is high.
5. When both the inputs are at 0V, both diodes are in reverse biased and hence do not conduct. The output is low.

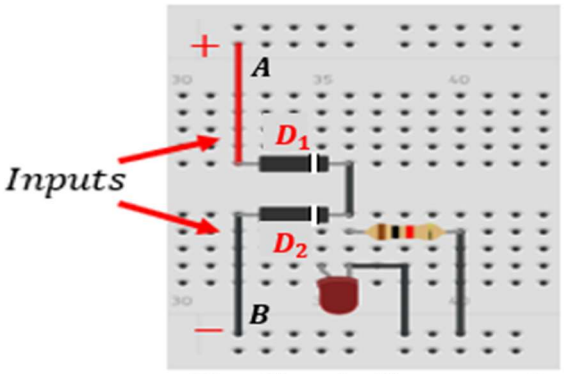


Fig: *Circuit diagram of OR gate*